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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	14

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/669,354	ISHIYAMA, HISANOBU	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 16-18* is/are allowed.

6)☒ Claim(s) *5-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed January 12, 2004 with respect to claims 5-15 have been fully considered but they are not persuasive. In response to Applicant's arguments (on claims 5 and 7) that reference Shimizu does not teach an internal delay circuit, the examiner disagrees. As shown in Fig. 3, Shimizu teaches the signal ENABLE E2 (display control signal) is output before the display control signal is fed back to the internal delay circuit 112a. In response to Applicant's arguments (on claims 8 and 12) that reference Shimizu does not teach "a selection terminal for selecting either a master or slave," the examiner disagrees. In fact, Shimizu teach the enable (display control signal) output of "1" is derived from the EO terminal of the first-stage X driver 3. Since the EI' signal is "0" in the other X drivers 4 to 6, the enable output is kept at "0" (disabled) (col. 8, lines 19-22). Thus, the first-stage driver 3 is set as master, display control signal is enabled, the display control signal is output to the next-stage driver, and display control signal is input to the internal delay circuit as cited above, while in other drivers (X drivers 4 to 6), which is set as slave, display control signal generation is disabled.

Allowable Subject Matter

2. Claims 1-4, 16-18 are allowed.

Reasons for Allowance

3. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination does not teach or suggest, an electro-optical device among other things, including each of the master IC and the at least one slave IC has an input terminal for receiving display control signal output from the display control signal generation section of the master IC through an external wiring.

The closest prior art, Shimizu (U.S. Patent No. 5,801,674) teaches an LCD device comprising a plurality of ICs, each of which has an input and an output terminal for receiving display control signal.

However, reference Shimizu does not teach the display control signal output from the master IC is also input to the master IC.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 5-8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu (U.S. Patent No. 5,801,674).

Referring to claims 5, 7, 8, and 12, Shimizu teaches a display device comprising a liquid crystal display panel having a plurality of scanning electrodes (second electrodes), a plurality of signal electrodes divided into a plurality of signal electrode groups (first electrodes), and liquid crystal elements arranged at intersections of the scanning electrodes and the signal electrodes; a controller (an external MPU) for outputting control signals including a start signal, enable signal and clock signal and display data; and a plurality of drivers supplied with the display data and the control signals including the start signal, enable signal and clock signal from the controller, for fetching the display data and selectively supplying the fetched display data to the plurality of

signal electrode groups (col. 2, lines 40-52). As shown in Fig. 1, the LCD display device as taught by Shimizu comprises a Y driver 2 (second driver) for driving the scanning electrodes and four X drivers 3, 4, 5, 6 (first driver) for driving four signal electrode groups obtained by dividing all of the horizontal signal electrodes in a horizontal direction are arranged in the peripheral portion of the LCD panel 1 (col. 3, lines 53-57). Shown in Fig. 2 is the internal structure of a single IC X driver 3 (master IC), wherein the data fetch starting signal and load signal are generated in the cascade connection control circuit 12 (a display control signal generation section) by decoding the SYNC signal (col. 4, lines 61-64). Each of the IC X driver has an input terminal EI together with the input circuit 11 for receiving control signals, and output terminal EO for generating control signal to the next-stage X driver through external wiring as shown in Fig. 1. Shimizu further teaches each of the X drivers starts to fetch data when the operation of the preceding-stage X driver is ended, and the operation thereof is effected for a period of time necessary for fetching data and then terminated (col. 4, lines 1-13). As shown in Fig. 3, Shimizu teaches the signal ENABLE E2 (display control signal) is output before the display control signal is fed back to the internal delay circuit 112a. Shimizu further teaches the enable (display control signal) output of "1" is derived from the EO terminal of the first-stage X driver 3. Since the EI' signal is "0" in the other X drivers 4 to 6, the enable output is kept at "0" (disabled) (col. 8, lines 19-22). Thus, the first-stage driver 3 is set as master, display control signal is enabled, the display control signal is output to the next-stage driver, and display control signal is input to the internal delay circuit as cited above, while in other drivers (X drivers 4 to 6), which is set as slave, display control signal generation is disabled.

In regard to claim 6, since the display control signals are different from each of the X drivers 3-6 depending on the input data, time delay in each driver is different from one another.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9-11, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (U.S. Patent No. 5,801,674) in view of S-MOS System, Inc., Dot Matrix LCD Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter S-MOS)

Referring to claims 9 and 13, as cited above, Shimizu teaches a selection circuit for enabling the next stage slave X driver 4 output from the master X driver 3 through the EO output terminal. Thus, Shimizu teaches all the limitations of claims 9 and 13, except that input/output capable of switching from outputting display control to inputting display control.

However, S-MOS teach a method for driving LCD, comprising a plurality of ICs, which can be configured to be a master IC or a slave IC as shown on page 15. In the table shown on page 22, the input/output switching state configuration is based on the control signal FR and the selection signal M/S for selecting master or slave state.

Therefore, it would have been obvious to one skilled in the art to utilize the teachings of S-MOS in combination with the method as taught by Shimizu in order to permit the user to implement high-performance handy systems operating from a miniature battery (page 5).

Referring to claims 10-11 and 14-15, although Shimizu does not teach using an AND or an OR gate for selecting master or slave IC. However, with reference again to the table on page 22, section 3.2.3.2 of the manual for driver SED 1520/21, the state of the driver (master or slave) depends on both the M/S signal and FR signal. Therefore, it is implied a combinational logic function using either AND or OR circuit to connect these two signals in order to switch the state of the IC.

Therefore, it would have been obvious to one skilled in the art to utilize the teachings of S-MOS in combination with the method as taught by Shimizu in order to permit the user to implement high-performance handy systems operating from a miniature battery (page 5).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

03/15/2004

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600